GIGAHERTZ BANDWIDTH MULTIBIT PHASE SAMPLING AND RECONSTRUCTION OF MICROWAVE SIGNALS

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ABSTRACT

This paper presents novel techniques for digitally sampling and reconstructing the phase of microwave signals. A practical implementation giving two bits of phase resolution and a one gigahertz bandwidth using silicon ECL and GaAs CDFL devices is described, outlining the constructional techniques developed to implement this high speed logic design. The performance observed is shown to be in agreement with computer simulations and future extensions to wider bandwidth and better phase resolution are discussed.

INTRODUCTION

Technological improvements in recent years have been offering the systems designer a steady improvement in digital processing speed and density. The implication is that digital signal processing is becoming the optimum solution in applications previously dominated by analogue techniques, and may offer better system performance. The improved speed and storage density of digital memories has made microwave signal storage with very long record durations and infinite storage possible. Increases in processing power are resulting from larger scales of integration, parallelism and higher operating speeds. Complex digital processing techniques are now becoming feasible for gigahertz bandwidth signals.

This paper looks at techniques of digitising and reconstructing microwave signals to facilitate coherent digital IF processing. The techniques discussed could find application in test equipment for microwave pulse analysis and synthesis as well as pulse systems for use in communications and EW.

THEORY

A block diagram for a typical phase sampler and reconstructor system is shown in figure 1. This mixes an incoming signal with a local oscillator to produce in-phase and quadrature baseband components. These are then sampled and quantised by a pair of analog to digital converters (A/Ds). On reconstruction the digital data is passed to a pair of digital to analog converters and mixed up with an SSB modulator to regenerate the frequency of the original signal. This digital representation of the signal may be represented on an Argand diagram as shown in figure 2. For pure phase sampling the valid data points are confined to a unit circle on the diagram. In the case of 2 bit phase sampling the A/Ds are simple comparators producing the four vectors shown on the diagram.

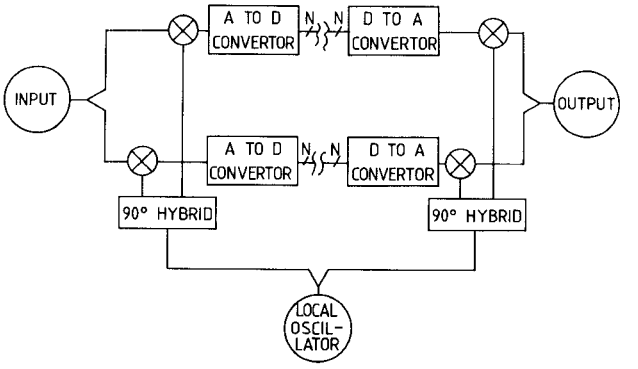

FIG 1 BLOCK DIAGRAM OF PHASE SAMPLER AND RECONSTRUCTOR

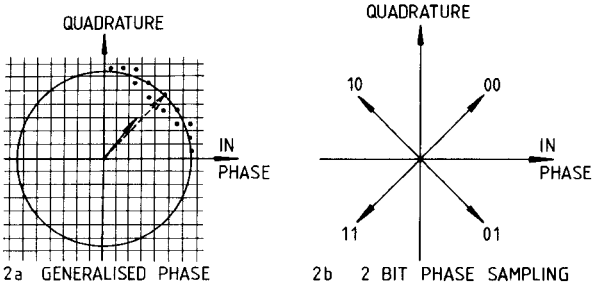

FIG. 2 REPRESENTATION OF PHASE SAMPLING ON THE ARGAND DIAGRAM

In order to implement sampling and reconstruction at fixed frequency gigabit rates with minimal complexity, delay line samplers have been developed as shown in figure 3. This reduces the maximum clock frequencies required in a system and automatically performs the first stage of multiplexing down to data rates compatible with conventional ECL logic. A similar technique can be applied to the reconstruction.

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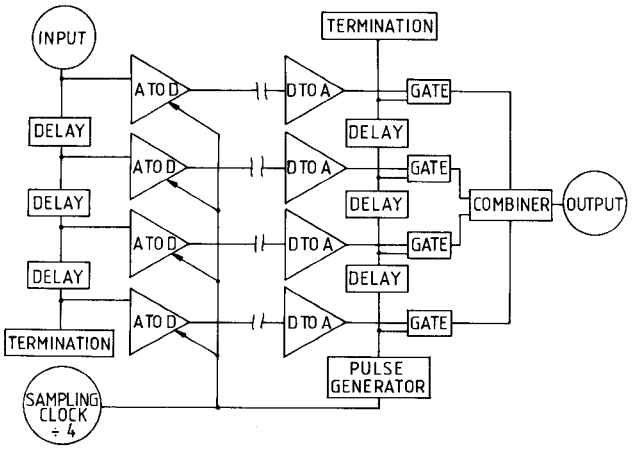

FIG. 3 BLOCK DIAGRAM OF A BASEBAND "DELAY LINE" SAMPLER AND RECONSTRUCTOR

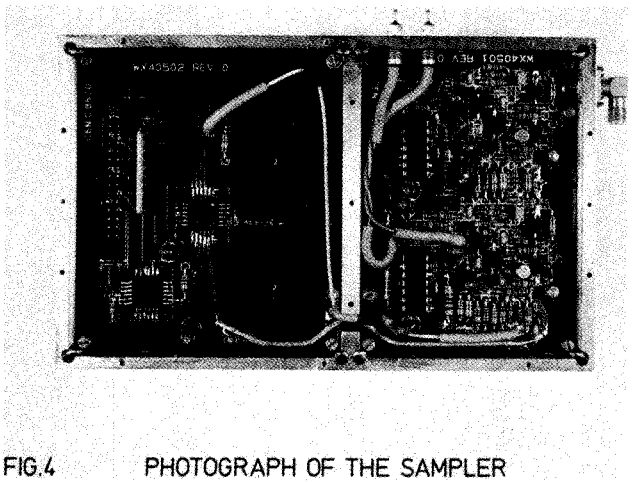

FIG. 4 PHOTOGRAPH OF THE SAMPLER

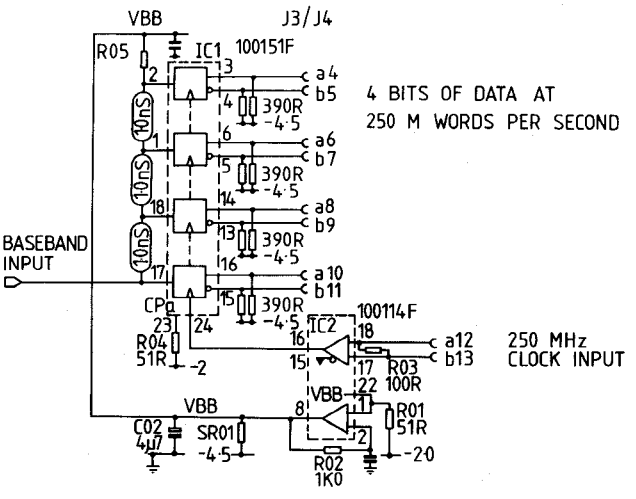

FIG. 5 CIRCUIT DIAGRAM OF THE SAMPLER

PRACTICAL SYSTEM CONSTRUCTION

This section describes a 1 GHz bandwidth, 2 bit phase sampler and reconstructor. A centre frequency of 3 GHz was used and the quadrature mixer was produced in microstrip. The 90 degree phase shifter and power splitter/combiners were implemented using a quarter wave line and Wilkinson networks respectively.

In-phase and quadrature baseband signals were one bit quantised by two sampler units of the type shown in figure 4. The signal is first amplified, level shifted and limited by a DC coupled amplifier to produce an ECL compatible signal. Figure 5 shows the circuit diagram of the delay line sampler. IC1 is a hex D type latch. The three delays are nominally 1ns but were adjusted (after testing a prototype) to compensate for errors in the D type clock alignment within the package or input propagation delay and the delay caused by the ECL input capacitance. A four bit word is driven differentially out via a DIN 41612 connector at 250 M words per second.

The connector consists of two rows, a and b, of 16 pins on an 0.1 inch pitch. By grounding the odd and even pins in rows a and be respectively the discontinuity was minimised. Measurements were made with a Time Domain Reflectometer having a 50ps risetime. The connector impedance was estimated at 65 ohms (a voltage reflection coefficient of 13%) producing reflections within the noise immunity of the devices used. When driven with ECL signals near end crosstalk was typically 30mV peak which was considered insignificant compared to the noise margin.

The reconstructor shown in figure 6 receives the digital data from one of the samplers via a similar connector. Clock and data signals are buffered by an ECL receiver, and the data is latched to another hex D type. The clock is buffered by a GaAs three input NOR gate to speed the transition times and is then gated with a delayed version of itself to produce a 1 ns low pulse from every rising edge. This pulse is used to select each data bit for 1 ns in turn using another GaAs quad NOR package, the outputs from which are combined in a wired OR gate. The multiplexed data stream is then level shifted by a discrete comparator which limits the signal to reduce clock breakthrough. Another band limited DC coupled amplifier removes unwanted high frequency components, and provides the drive to the output quadrature mixer.

Both circuits were fabricated on multilayer fibreglass substrates, an example of which is shown in figure 7. The rise times of GaAs logic require the use of matched transmission lines and low inductance terminations, while the circuit complexity makes conventional microstrip impractical. The six layer board shown is a double sided microstrip with an internal stripline interconnect layer. All the delay elements used in the designs were microstrip lines alternating between the two sides of the board to avoid the capacitive fringing effects of meander lines which were found to be significant. Transmission lines on different levels were interconnected by

means of conventional plated through holes which produced negligible discontinuities.

PERFORMANCE

The testing of the sampler and reconstructor presents problems in that new techniques have to be developed to enable accurate in circuit measurement. To evaluate input offset and sampling alignment an HPIB controlled synthesiser was used as a discretely swept frequency source applied both to the sampler clock and via a delay line to the signal input. This effectively sweeps the signal zero crossings with respect to the sample clock transitions along the sampler delay line. By plotting the states of each of the sampler outputs against the input frequency it is possible to deduce the lengths of the internal delays, the random sampling jitter, input offset and minimum drive level. The delays were found to be accurate to ± 100ps, random jitter was less than 20ps, the input offset was less than 30 mV and the minimum drive level was -20 dBm.

The testing of the reconstructor requires a 250 MHz 4 bit word generator and a high speed sampling scope. The word generator was designed and built in house since no suitable equipment is available commercially. Waveform traces and eye

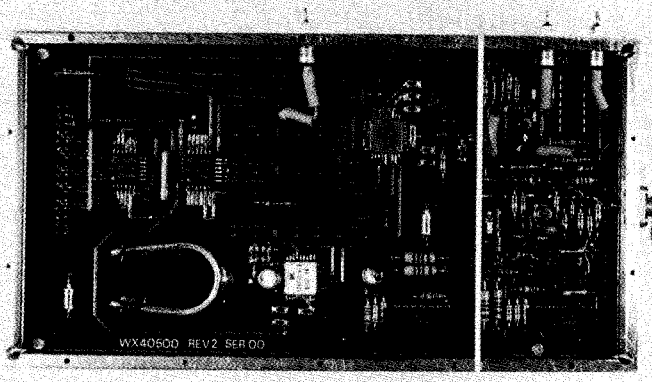

FIG.6 PHOTOGRAPH OF THE MULTIPLEXER (RECONSTRUCTOR)
1 G BIT/SEC

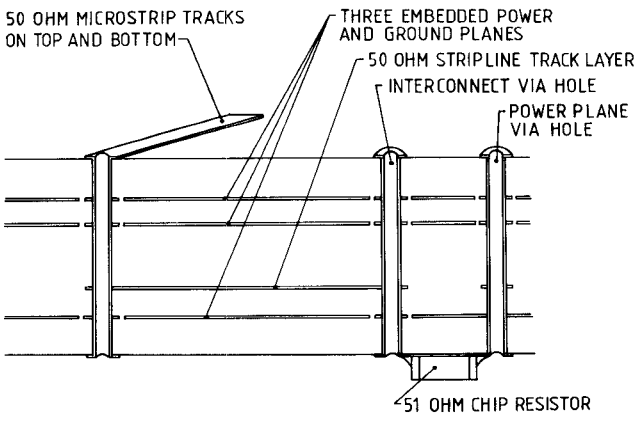

FIG. 7 CROSS-SECTION OF A SIX LAYER FIBREGLASS PCB (NOT TO SCALE)

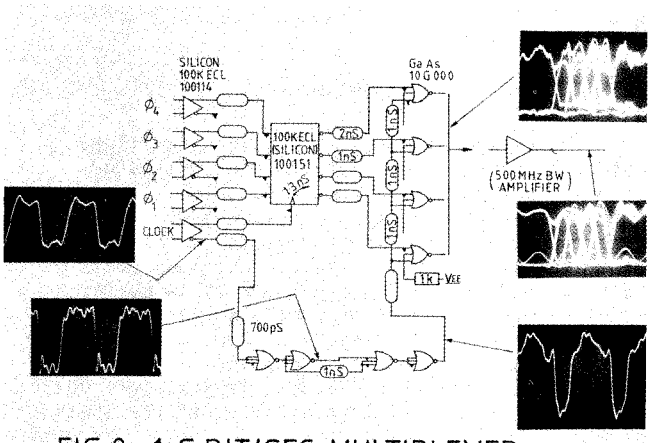

FIG.8. 1 G BIT/SEC MULTIPLEXER

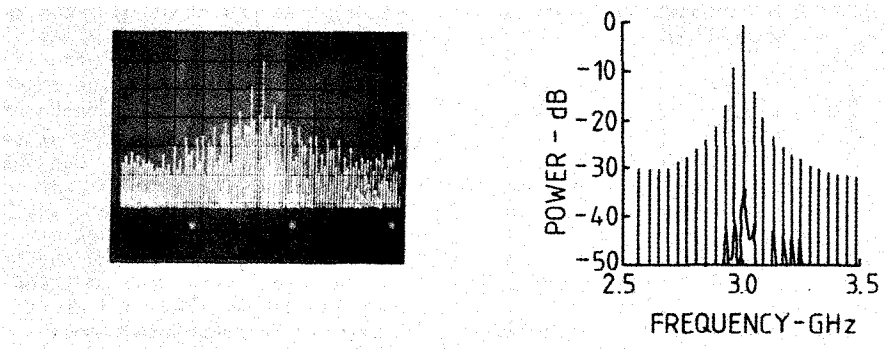

FIG.9

diagrams measured using an 18 GHz bandwidth sampling scope are shown in the circuit diagram figure 8.

The validity of the phase sampling theory and proof of the full system performance is confirmed by the spectra in figure 9. This compares the spectra of a signal which has passed through the sampler reconstructor system as compared against a computer simulation of the quantisation spurii. The results show a good correspondence over the 1 GHz band of operation.

EXTENSIONS

The techniques described in this paper could be extended to allow more bits of resolution. It could for example extend the sampling capability of a silicon 6 bit 200 MHz A to D to 1 GHz by using a 5 way delay line multiplexer. This would need a sample and hold of sufficiently small aperture but could lead to a phase resolution of about 1 degree. It also lends itself to irregular sampling at high rates since the sample intervals may be accurately controlled by the delay lines and matched exactly on reconstruction.

CONCLUSION

The design produced by the authors illustrates the problems encountered when utilising high speed digital integrated circuits such as GaAs in subsystem design. It also shows innovative use of circuit trace propagation delays as enhancements to the processing functions available instead of treating them purely as device interconnects. The techniques discussed are applicable to any high speed microwave modulation measurement or generation equipment. This permits the multibit digital processing of data in 1 GHz bandwidths using readily available off the shelf devices.